

WHAT IS CLAIMED IS:

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1. A circuit arrangement comprising:
a complementary pass transistor logic;
a static driver connected to the
complementary pass transistor logic and driving
10 complementary input nodes to each other of the
complementary pass transistor logic by a low swing
voltage; and
a charge recycling circuit connected to the
complementary pass transistor logic and performing
15 charge sharing between the complementary input nodes
when the complementary pass transistor logic is not
driven by the static driver.

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2. The circuit arrangement as claimed in claim
1, wherein a swing level of the low swing voltage ranges
from a ground voltage level to a supply voltage level
25 minus a threshold voltage level.

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3. The circuit arrangement as claimed in claim
1, the static driver is formed of a plurality of
transistors connected in series.

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4. A low swing charge recycling circuit

arrangement comprising:

5 a complementary pass gate stage having driving inputs to receive each of driving input signals, having complementary outputs to produce an output signal on one hand and a complementary output signal on the other and determining a logic operation of the circuit arrangement;

10 a static low swing driver stage having a signal input to receive an input signal, having a clock input to receive a clock signal, and having complementary outputs to produce low swing complementary signals to each output to be provided to the driving inputs of the complementary pass gate when the clock signal is in one of two states; and

15 an equalization stage being connected to the complementary outputs, having a clock input to receive the clock signal and producing complementary signals to the driving inputs of the complementary pass gate stage when the clock signal is in the other state, whereby
20 a charge shared signal of an intermediate voltage level between those of the complementary outputs is shared between the driving inputs.

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5. An adder comprising:

30 a carry propagating circuit for alternatively propagating low swing driven complementary carry input signals and charge sharing complementary carry input signals;

a static low swing driver circuit receiving generate signals and producing low swing driven complementary generate signals;

35 a pass gate network receiving the complementary carry input signals, the complementary generate signals and propagate signals and being

controlled by the propagate signals for producing a
sum signal by applying XOR operation to the complementary
carry signals with the propagate signals;

an equalization circuit adapted to be
5 operative alternatively with the static low swing driver
circuit and providing charge sharing complementary
generate signals to the pass gate network; and

a latch circuit connected to the pass gate
network and latching the produced sum signal.

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6. An adder module comprising:

15 at least one adder connected in series, each
adder being provided on the basis of one bit to be added;
and

a carry input signal equalization circuit
receiving carry input signals and providing charge
20 sharing complementary carry input signals to one end
of the adders connected in series,

wherein the adder includes:

a carry propagating circuit for alternatively
propagating low swing driven complementary carry input
25 signals and the charge sharing complementary carry input
signals;

a static low swing driver circuit receiving
generate signals and producing low swing driven
complementary generate signals;

30 a pass gate network receiving the
complementary carry input signals, the complementary
generate signals and propagate signals and being
controlled by the propagate signals for producing a
sum signal by applying XOR operation to the complementary
35 carry signals with the propagate signals;

an equalization circuit adapted to be
operative alternatively with the static low swing driver

circuit and providing charge sharing complementary
generate signals to the pass gate network; and
a latch circuit connected to the pass gate
network and latching the produced sum signal.

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7. The adder module as claimed in claim 6
10 further comprising:
a carry propagating path for propagating the
complementary carry input signals in series of bits;
a carry skip path bypassing the adders
connected in series in order to pass the complementary
15 carry input signals transparently; and
a carry conflict-free circuit for protecting
a conflict of the propagated carry input signals and
the passed carry input signals.

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